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NOTICE OF ALLOWANCE AND ISSUE FEE DUE

TM31/1011

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APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
08/905,356	08/04/97	074	NGUYEN, T 2187	10/11/00
First Named Applicant: BELGARD,			35 USC 154(b) term ext. = 0 Days.	

TITLE OF INVENTION: ADDRESS TRANSLATION MECHANISM AND METHOD IN A COMPUTER SYSTEM

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 RAB-97-002	711-213.000	T58	UTILITY	YES	$620.00	01/11/01

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
B. If the status is the same, pay the FEE DUE shown above.

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B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number.
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/905,356	08/04/97	BELGARD R	RAB-97-002

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EXAMINER	
NGUYEN, T	
ART UNIT	PAPER NUMBER
2187	17

DATE MAILED: 10/11/00

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to 8/18/00.

☒ The allowed claim(s) is/are 38-53, 55-112.

☐ The drawings filed on _____ are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR REPLY to comply with the requirements noted below is set to EXPIRE **THREE MONTHS** FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☒ Applicant MUST submit NEW FORMAL DRAWINGS

☒ because the originally filed drawings were declared by applicant to be informal.

☐ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____.

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any reply to this notice should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☒ Examiner's Statement of Reasons for Allowance

DETAILED ACTION

1. This is a response to the amendment, filed 8/18/00.

2. Claim 54 has been canceled. Claims 38-53,55-112 remain pending.

3. Claims 38-53,57-112 were previously allowed. Claim 54 was rejected. Claims 55 and 56 were objected to but would be allowable if rewritten to incorporate the limitations of claim 54.

4. Applicant has amended claims 57,82 as suggested by Examiner. The objections to these claims are withdrawn.

5. Applicant has rewritten claims 55 and 56 as independent claims and incorporating all the limitations of claim 54. Thus claims 55 and 56 are now allowable.

Allowable Subject Matter

6. Claims 38-53,55-112 are allowable.

7. The following is an examiner's statement of reasons for allowance:

8. As to claims 38,61,66 the prior art of record does not teach generating an actual physical address from a virtual address, the virtual address having both a segment identifier and a segment offset by calculating a linear address based on the entire virtual address, and by calculating the physical address based on the calculated linear address; and generating a fast physical address before the actual physical address is generated.

9. Claims 39-42 are also allowed for incorporating the limitations of claim 38, and further limitations.

10. Claims 62-65 are also allowed for incorporating the limitations of claim 61, and further limitations.

11. Claims 67-69 are also allowed for incorporating the limitations of claim 66, and further limitations.

12. As to claim 43 the prior art of record does not teach converting a first virtual address having both a segment identifier portion and a segment offset portion to a first linear address, the first linear address being based on all portions of the virtual address generating the tentative physical address before the converting the first linear address to a first physical address.

13. Claims 44-48 are also allowed for incorporating the limitations of claim 43, and further limitations.

14. As to claim 49, the prior art of record does not teach nor suggest a first operation for converting virtual addresses having both a segment identifier portion and a segment offset portion to linear addresses, such that both the segment identifier and segment offset portions of the virtual addresses are used for converting the linear addresses and generated the fast physical addresses before the virtual addresses are converted in the first operation.

15. Claims 50-53 are also allowed for incorporating the limitations of claim 49, and further limitations.

16. As to claim 55, the prior art of record does not teach nor suggest the a virtual to linear address converter circuit for generating a calculated linear address based on a virtual address, the virtual address having both a segment identifier and a segment offset, and the calculated linear

address being based on all of the virtual address and a linear to physical address converter for generating a calculated physical address based on the calculated linear address, the calculated physical address including a calculated page frame and a calculated page offset; and

a fast physical address circuit for generating a fast physical address including a fast page frame and a fast page offset;

wherein a memory reference can be generated based on the fast physical address;

further wherein the fast physical address is based on linear address information relating to the virtual address and physical address information relating to a prior virtual address.

17. As to claim 56, the prior art of record does not teach nor suggest the a virtual to linear address converter circuit for generating a calculated linear address based on a virtual address, the virtual address having both a segment identifier and a segment offset, and the calculated linear address being based on all of the virtual address and a linear to physical address converter for generating a calculated physical address based on the calculated linear address, the calculated physical address including a calculated page frame and a calculated page offset; and

a fast physical address circuit for generating a fast physical address including a fast page frame and a fast page offset;

further wherein the virtual address is partially converted to a linear address by the fast physical address circuit and is combined with physical address information relating to a prior virtual address to generate the tentative physical address.

18. As to claim 57, the prior art of record does not teach nor suggest performing address translations which is done using a first operation to convert a first virtual address having both a segment identifier portion and a segment offset portion to a first linear address, such that all portions of the virtual address are considered when converting said virtual address into the first linear address and a second operation to convert the first linear address to a first physical address, and generating, in a first operation, a first virtual address, storing prior physical address information generated during a prior address translation; wherein a fast physical address can be generated based on the prior physical address information and the fist linear address before the converting the first linear address to a first physical address.

19. Claims 58-60 also allowed for incorporating the limitations of claim 57, and further limitations.

20. As to claim 70, the prior art of record does not teach nor suggest generating tentative memory references based on the virtual addresses; and converting the virtual addresses to linear addresses during segmentation operation, the linear addresses being based on translating all portions of the virtual address; and converting the linear addresses to physical addresses during a paging operation, so that actual memory references can be made based on the physical addresses; wherein the tentative memory reference can be generated while the virtual addresses are being converted in the first operation into the linear addresses.

21. Claims 71-73 are also allowed for incorporating the limitations of claim 70, and further limitations.

22. As to claim 74, the prior art of record does not teach a method including the steps of: converting a portion of the virtual address into a partial linear address; and combining the partial linear address with physical address information obtained from a prior memory reference to generate the fast physical address; generating a memory reference based on the fast physical address; converting the virtual address into an actual physical address during the time the linear address is also calculated based on both the segment id and segment offset of the virtual address; canceling the memory reference if the fast physical address and actual physical address are different.

23. Claims 75-76 are also allowed for incorporating the limitations of claim 74, and further limitations.

24. As to claim 77 the prior art of record does not each nor suggest a method comprising the steps of : generating a first calculated linear address based on a first virtual address in a first operation, the linear addresses being based on translating all portions of the first virtual address; and generating a fast physical address in a second operation, the fast physical address including linear address information relating to the first virtual address; and generating a first calculated physical address in a third operation based on the first calculated linear address; wherein the fast physical address is generated prior to the generation of the first calculated physical address.

25. Claims 78-81 are also allowed for incorporating the limitations of claim 77, and further limitations.

26. As to claim 82, the prior art does not teach nor suggest a system comprising: means for performing an address translation by generating a first physical address form a first virtual address by first calculating a first linear address based on both a first segment identifier and first offset associated with the first virtual address, such that all of the first virtual address is translated, and then calculating the first physical address based on the first calculated linear address; and a fast physical memory access circuit for generating a fast memory reference, which fast memory reference is based on physical address information from said address translation means; a bus interface circuit for initiating a fast memory access to a memory subsystem based on the fast memory reference.

27. Claims 83-85 are also allowed for incorporating the limitations of claim 82, and further limitations.

28. As to claim 86, the prior art of record does not teach nor suggest a method comprising the steps of: generating computed physical addresses by converting virtual addresses having a segment identifier and a segment offset into linear addresses, such that all portions of the virtual addresses are translated, and then converting the linear addresses into physical addresses; generating a speculative physical address based on the computed physical addresses; initiating a speculative memory access based on the speculative physical address.

29. Claims 87-88 are also allowed for incorporating the limitations of claim 86, and further limitations.

30. As to claim 89, the prior art of record does not teach nor suggest a system comprising: a virtual to linear address converter circuit for generating a first calculated linear address based on translating all portions of the first virtual address including a segment identifier and a segment offset; and a linear to physical address converter circuit for completing the first address translation by generating a first calculated physical address based on the first calculated linear address, the first calculated physical address including a first calculated page frame and a first calculated page offset; and wherein the system uses information from the first address translation during the second address translation so that the second address translation can be performed faster than the first address translation.

31. Claims 90-94 are also allowed for incorporating the limitations of claim 89, and further limitations.

32. As to claim 95, the prior art of record does not teach nor suggest a circuit including: an address generator for performing a first address translation of a first virtual address having an associated first segment identifier and a first offset, the first translation including converting all of the virtual address into a first linear address; the address generator also performing a fast address translation of a second virtual address having an associated second segment identifier and a second offset, said fast address translation occurring without converting all of the second virtual address into a second linear address; wherein the address generator uses information from the first address translation during the fast address translation so that the translation of the second virtual address takes less time than the first address translation.

33. Claims 96-100 are also allowed for incorporating the limitations of claim 95, and further limitations.

34. As to claim 101, the prior art of record does not teach nor suggest a method including the steps of: generating a first calculated physical address based on a first virtual address in a first operation, the first virtual address including a first segment identifier and a first offset and wherein the first operation converts all of the virtual address into a first linear address; and generating a second fast physical address in a second operation based on a second virtual address. the second virtual address including a second segment identifier and a second offset, and the second fast physical address being generated based on information obtained during the first operation, and without converting all of the second virtual address into a second linear address; wherein the second operation is performed faster than the first operation.

35. Claims 102-106 are also allowed for incorporating the limitations of claim 101, and further limitations.

36. As to claim 107, the prior art of record does not teach nor suggest the method including the steps of: performing a first address translation by translating a first linear address based on a first segment identifier and first offset associated with the first virtual address wherein all of the virtual address is translated; and calculating the first physical address based on the first calculated linear address and performing a second address translation using information obtained during said first address translation to translated a second virtual address into a second physical address, said second physical address being obtained without converting all of the second virtual address into a

second linear address; wherein the second translation can be achieved in less time than the first translation.

37. Claims 108-112 are also allowed for incorporating the limitations of claim 107, and further limitations.

38. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Drawings

39. The application having been allowed, formal drawings are required in response to this Office action.

Conclusion

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is (703) 305-3866.

41. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Than Nguyen
October 5, 2000